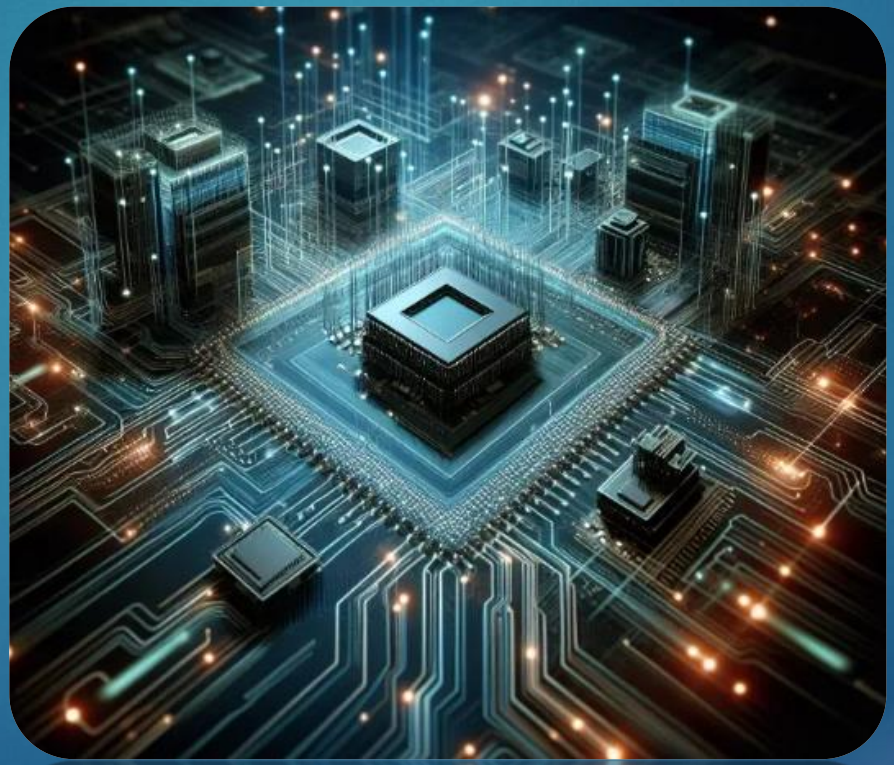
In the name of God

Computer Architecture

S.Ali.Zendehbad

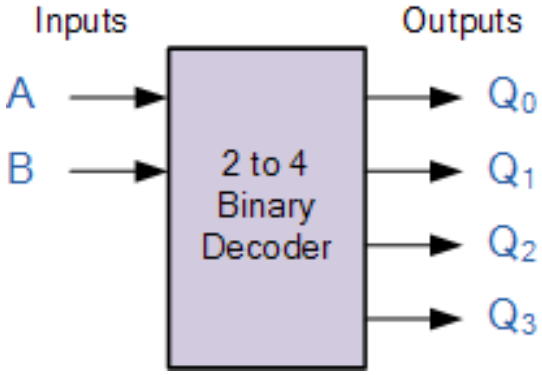


What was discussed in the previous weeks

- Technology Trends
- ISA
- Performance
- Benchmark
- Power Consumption and Its Impact on Technology

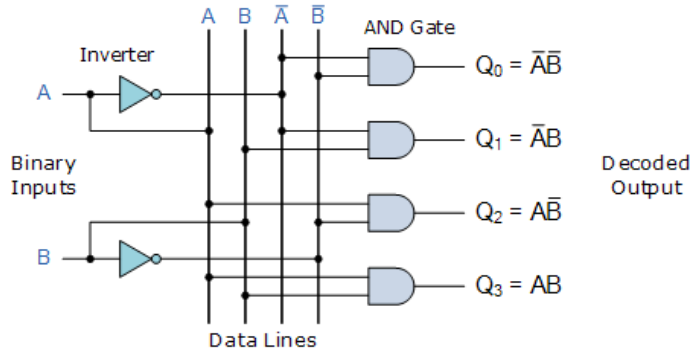
Overview of Logic Circuits

Combinational logic circuits are a function of only the current state of the input. As the input changes, the output changes instantaneously, which may be a logical 0 or a logical 1.

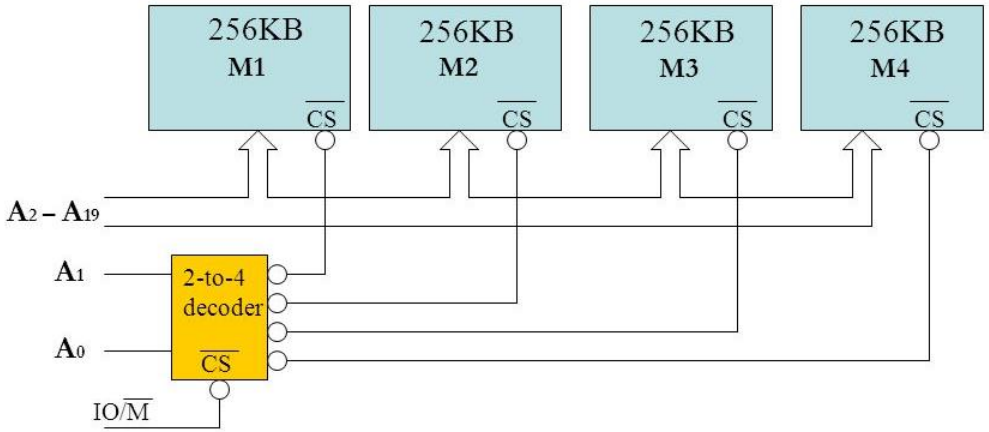


Truth Table

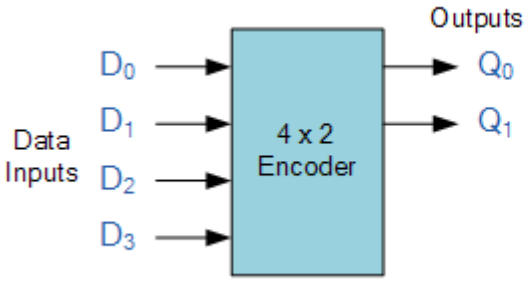
A	B	Q_0	Q_1	Q_2	Q_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



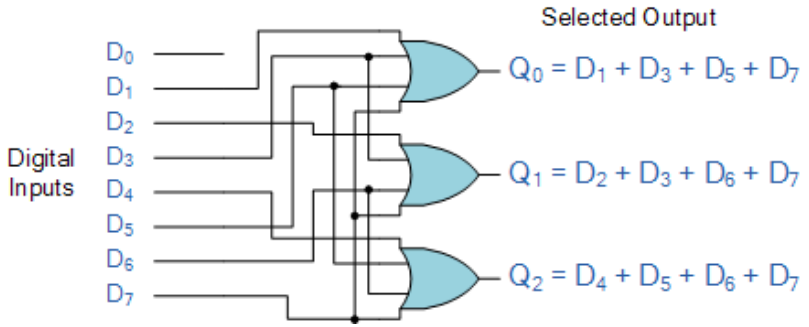
Application

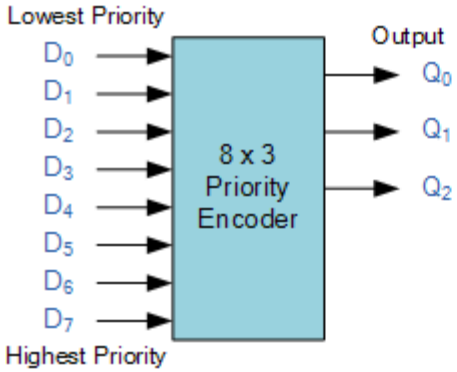


Combinational Logic



Inputs				Outputs	
D_3	D_2	D_1	D_0	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1
0	0	0	0	x	x

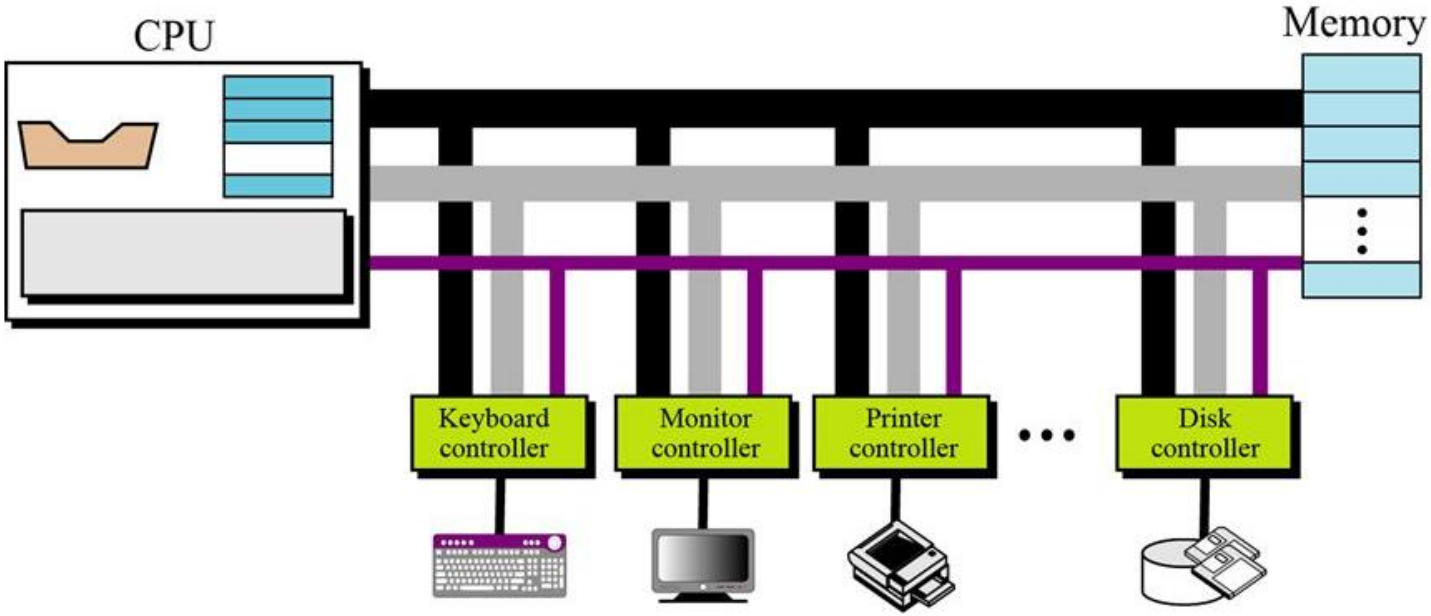




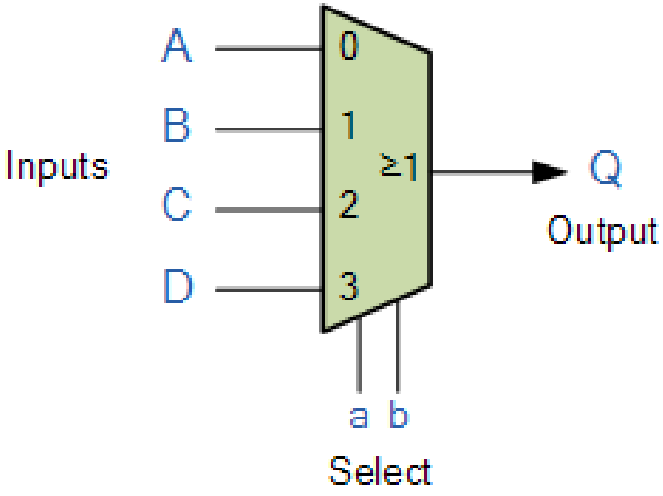
Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

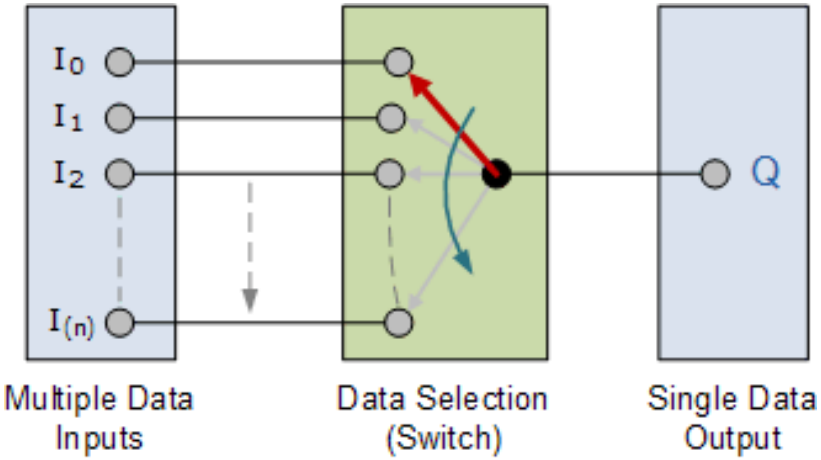
X = dont care

Application

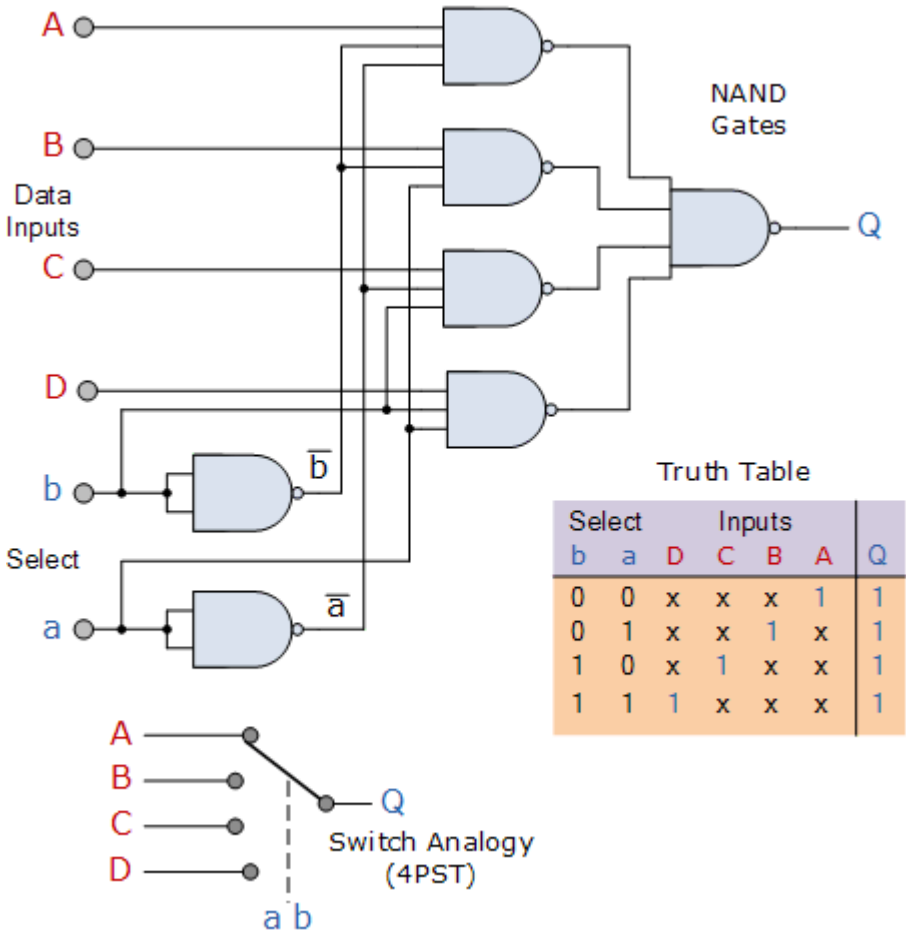


Combinational Logic





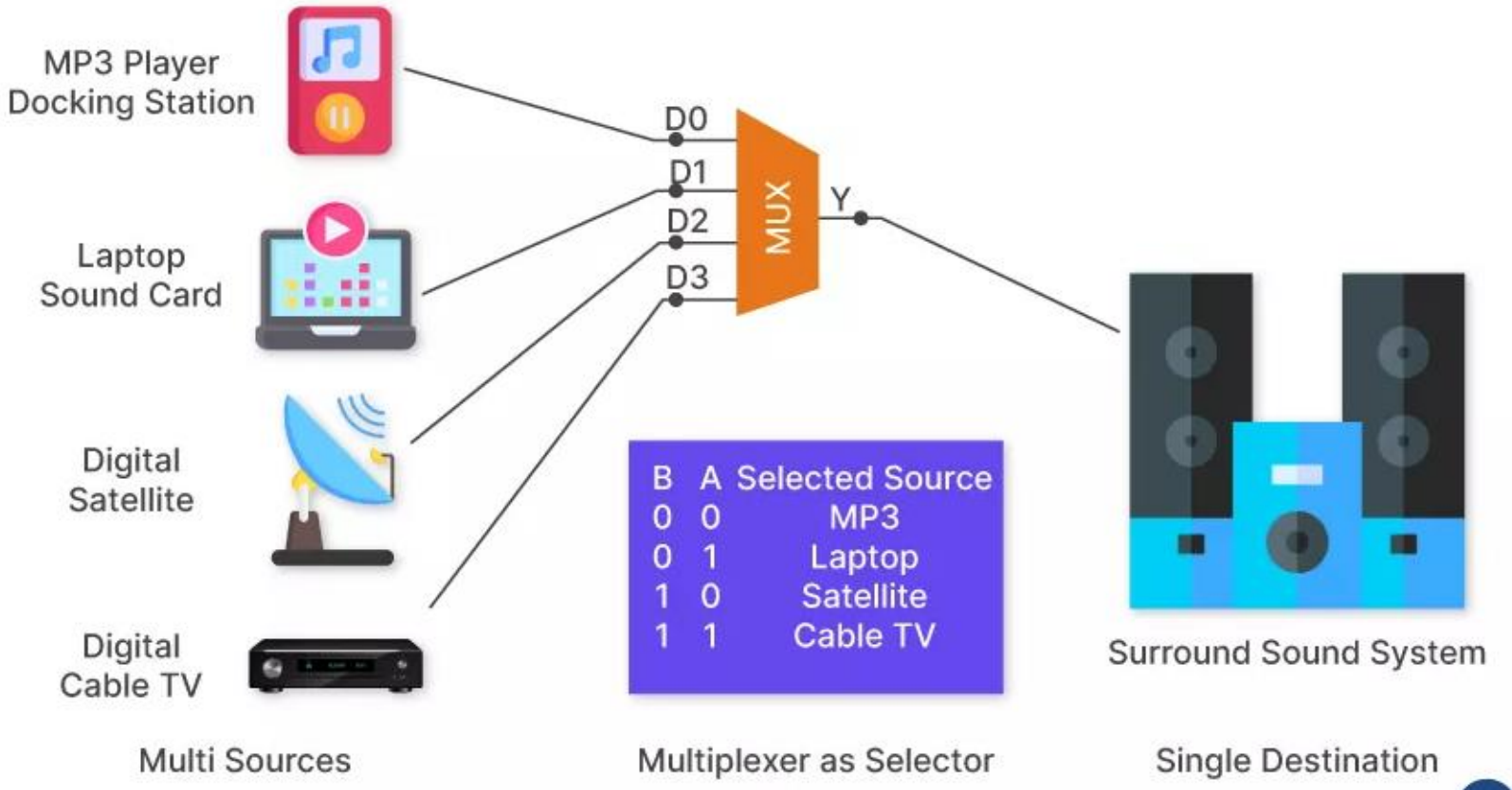
Combinational Logic



Truth Table

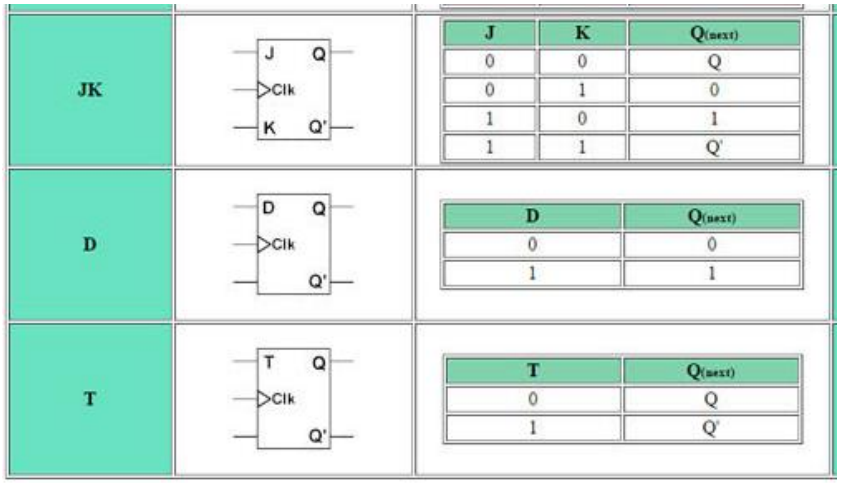
Select		Inputs				
b	a	D	C	B	A	Q
0	0	x	x	x	1	1
0	1	x	x	1	x	1
1	0	x	1	x	x	1
1	1	1	x	x	x	1

Application



Overview of Logic Circuits

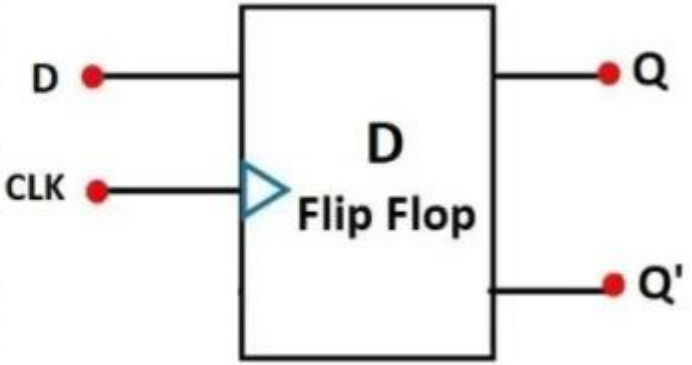
In **Sequential logic circuits**, the output value at any given moment is based on the current state of the inputs, and is also dependent on the previous state of the outputs. Such circuits are also referred to as "memory".



D Flop-Flop (Data)

Truth Table of DFlip Flop

D	CLK	Q	Q`
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0



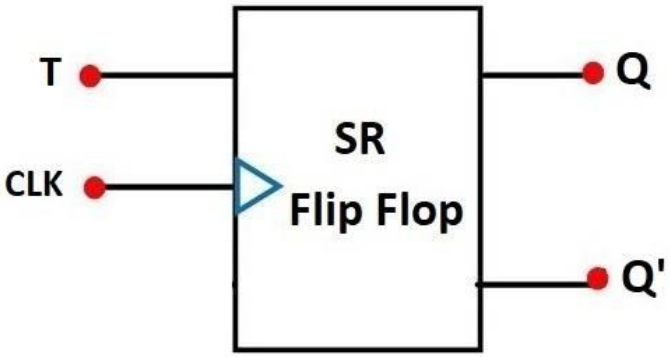
T Flop-Flop (Toggle)

Truth table			
CLK	T	Q_{next}	Comment
Rising edge	0	Q	Hold state
Falling edge	0	Q	Hold state
Rising edge	1	$\overline{Q}$	Toggle
Falling edge	1	Q	No change

Q_{next} - "after the clock transition" output

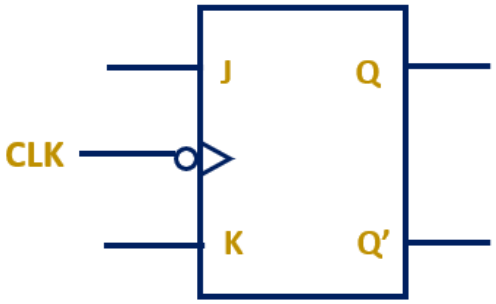
Q - the current output

Truth Table of T Flip Flop



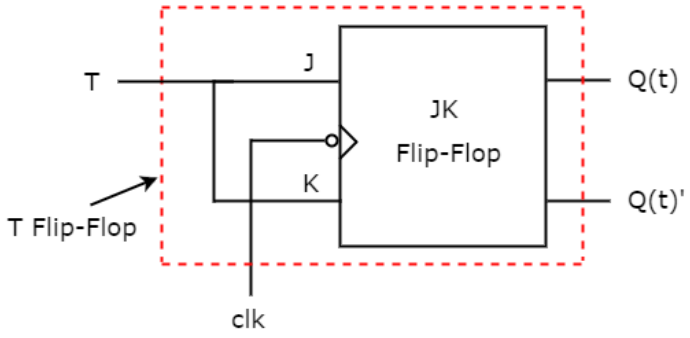
JK Flop-Flop (Jump&Kill)

Symbol

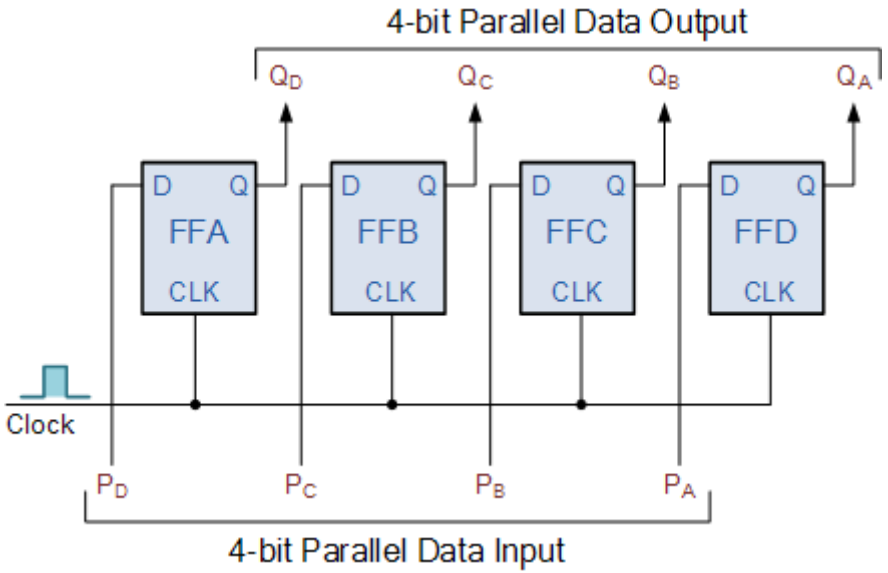


Truth Table

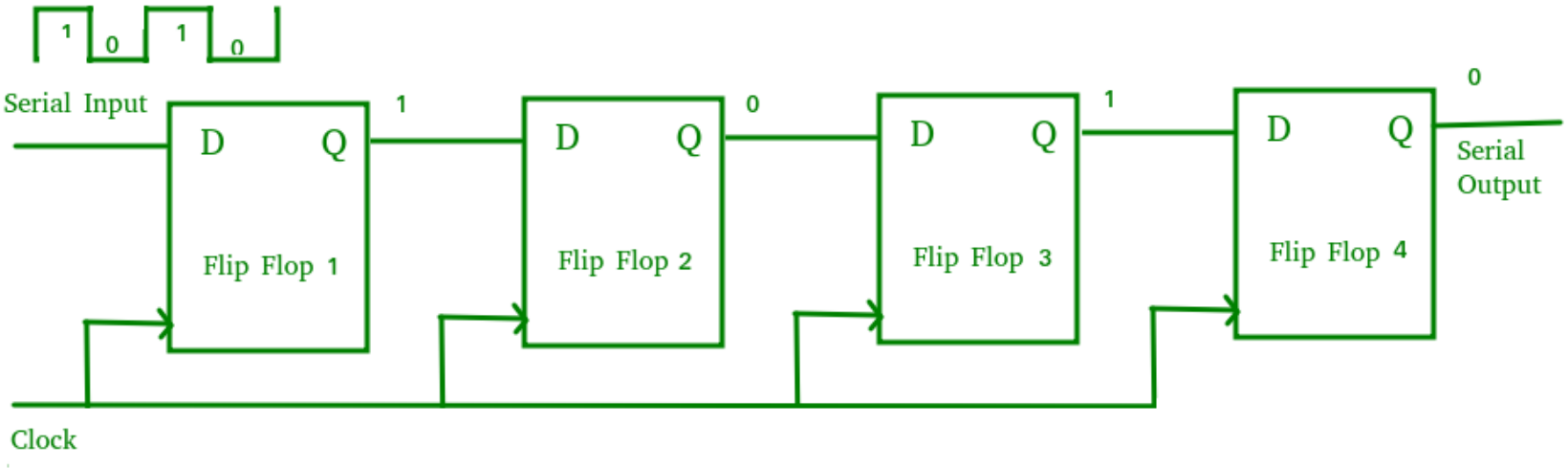
CLK	J	K	Q n+1
↓	0	0	Q n
↓	0	1	0
↓	1	0	1
↓	1	1	Q n'



Register

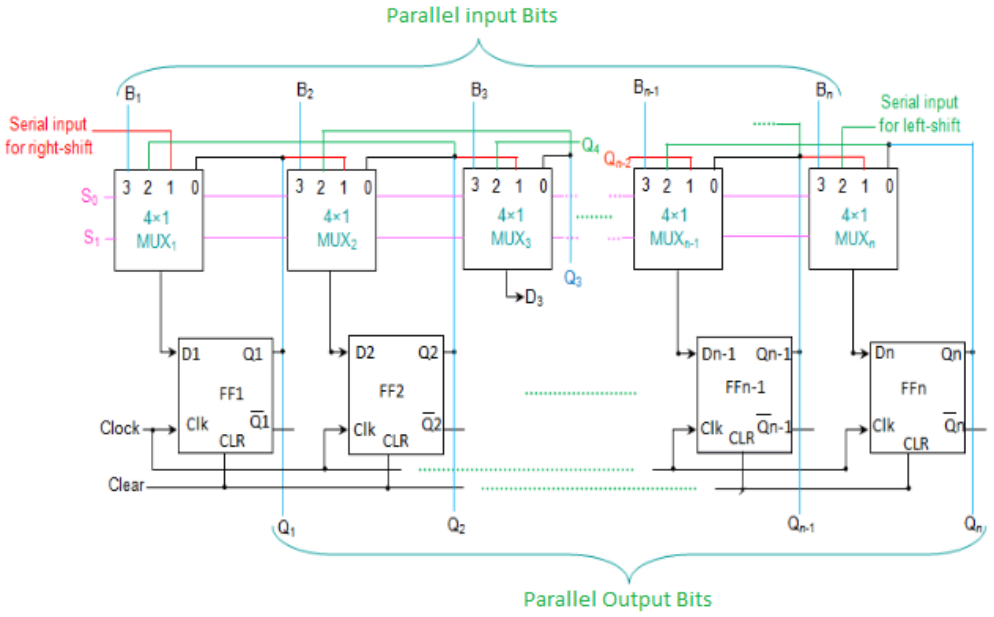

4-bit Parallel Data Output
Q_D
Q_C
Q_B
Q_A
D Q
FFA
CLK
D Q
FFB
CLK
D Q
FFC
CLK
D Q
FFD
CLK
Clock
P_D
P_C
P_B
P_A
4-bit Parallel Data Input

Shift Register



Universal Shift Register

S_1	S_0	Register operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

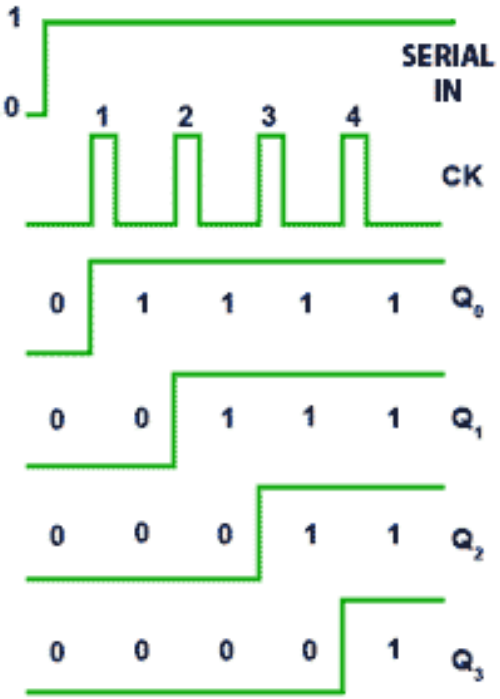


Application

State Table

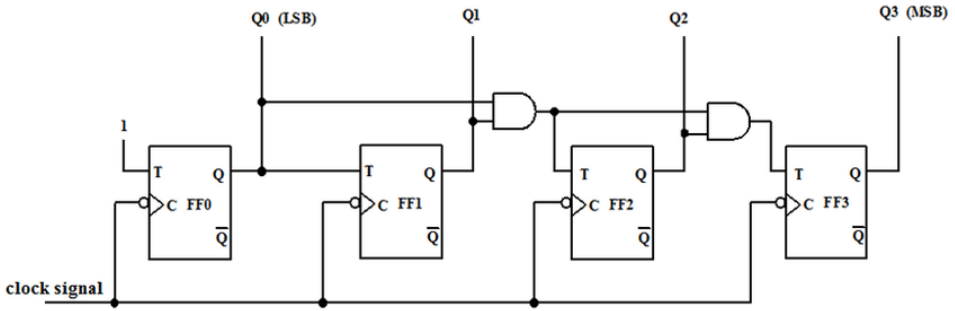
	After CK Pulse				
	0	1	2	3	4
Q_0	0	1	1	1	1
Q_1	0	0	1	1	1
Q_2	0	0	0	1	1
Q_3	0	0	0	0	1

Timing Diagram

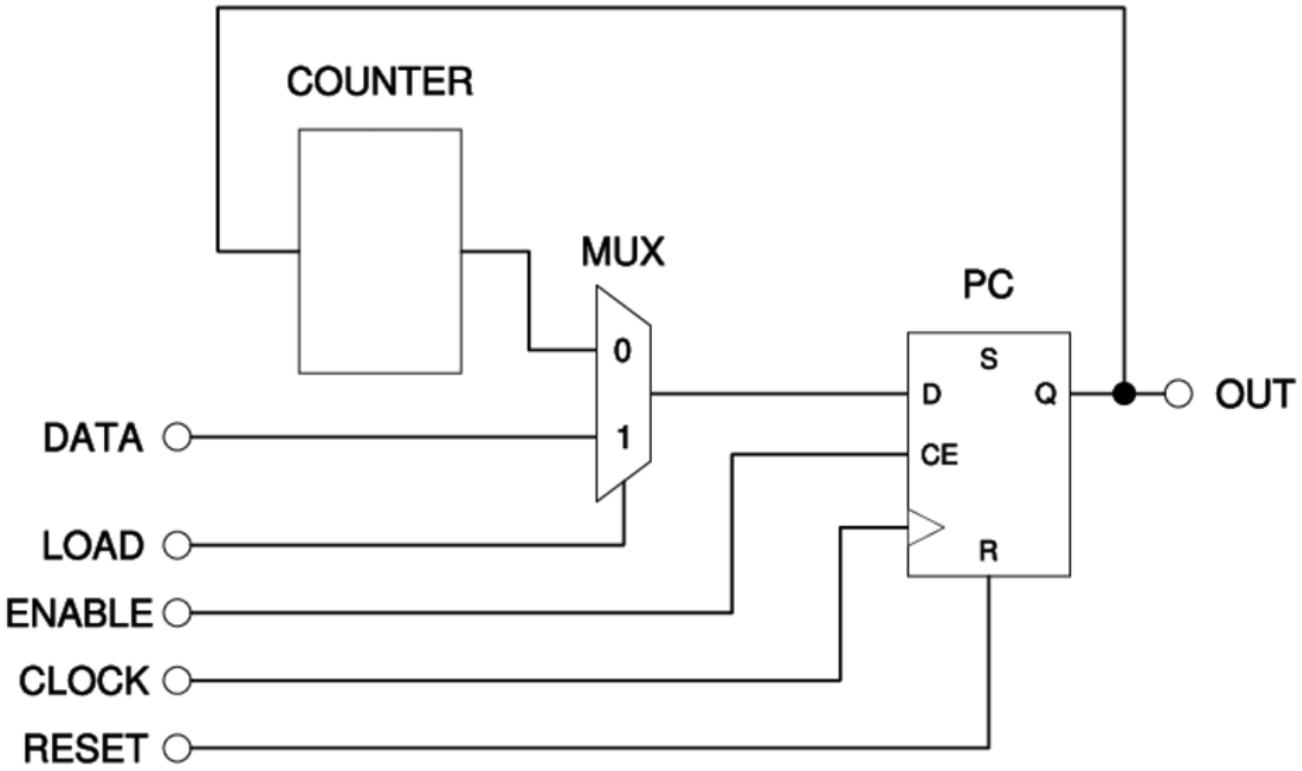


Counter

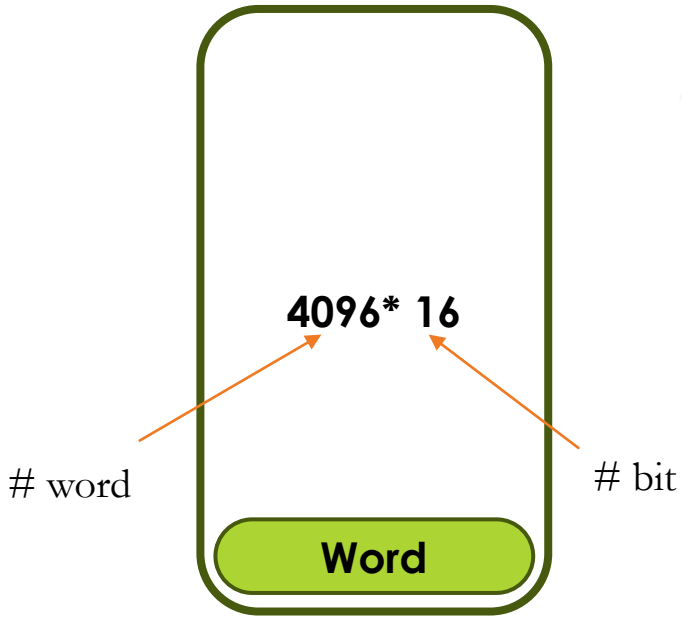
CLK	D	C	B	A	Output of reset logic Y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
–	1	0	1	0	0
–	1	0	1	1	0
–	1	1	0	0	0
–	1	1	0	1	0
–	1	1	1	0	0
–	1	1	1	1	0

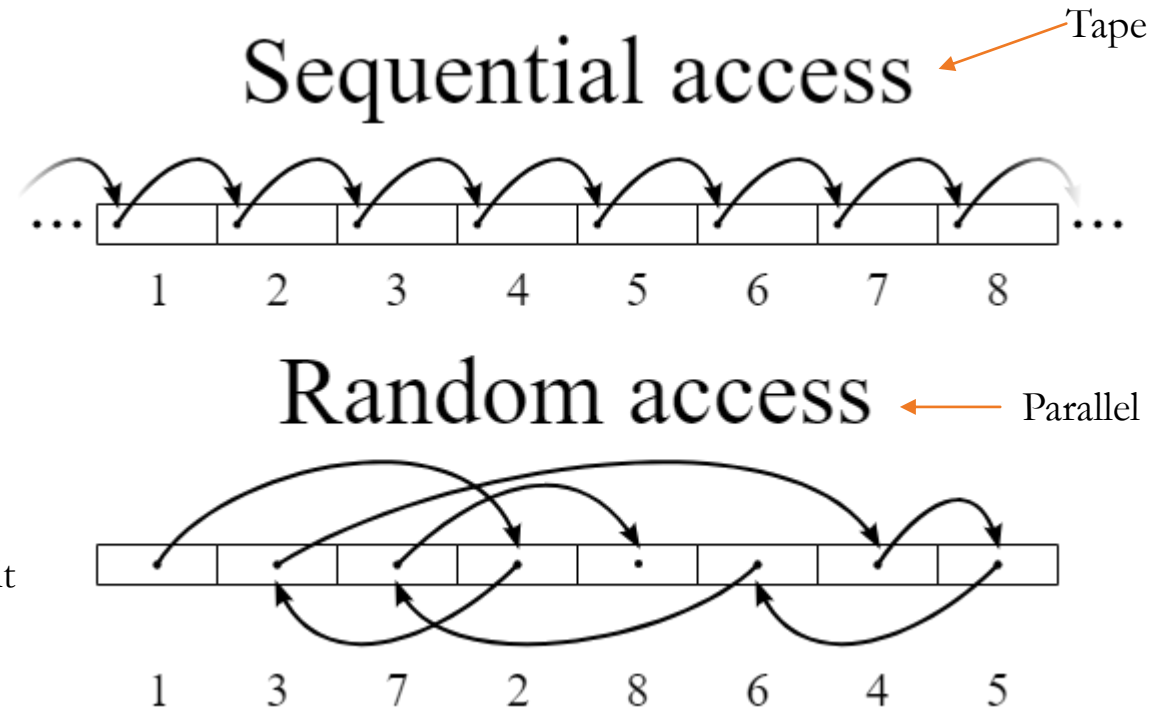


Program Counter (PC)

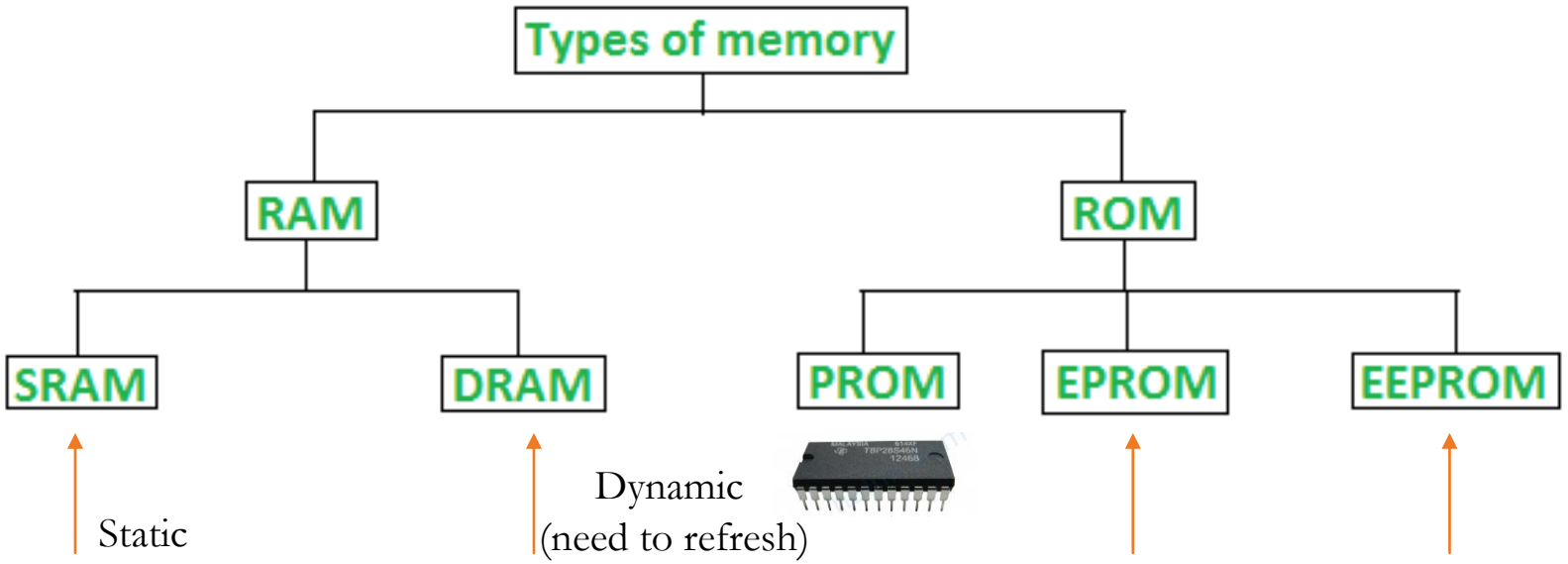


Memory


4096* 16
word
bit
Word


Sequential access
Tape
1 2 3 4 5 6 7 8
Random access
Parallel
1 3 7 2 8 6 4 5

Random Access



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